What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a memory cell array including a plurality of memory cells arranged in a column direction and a row direction,

wherein the memory cell array further includes:

a plurality of source line diffusion layers each of which is formed by connecting part of the memory cells in the row direction;

a plurality of bitline diffusion layers;

a plurality of isolation regions each of which divides one of the bitline diffusion layers; and

a plurality of word gate common connection sections;

wherein each of the memory cells includes one of the source line diffusion layers, one of the bitline diffusion layers, a channel region disposed between the source line diffusion layer and the bitline diffusion layer, a word gate and a select gate disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region;

wherein each of the bitline diffusion layers is disposed between two of the word gates which are adjacent to each other in the column direction;

wherein each of the word gate common connection sections is disposed above at least one of the isolation regions and connects the two adjacent word gates; and

wherein a plurality of word gate wiring layers are formed above the word gate common connection sections, each of the word gate wiring layers is connected to at least one word gate interconnection which is connected to one of the word gate common connection sections.

2. The nonvolatile semiconductor memory device as defined in claim 1,

wherein two of the word gates are respectively provided on both outer sides of two of the select gates which are adjacent to each other in the column direction, and the two word gates are connected by one of the word gate common connection sections.

3. The nonvolatile semiconductor memory device as defined in claim 2,

wherein each of the word gate common connection sections includes an insulator which covers the two adjacent select gates, and a conductor which is disposed on the insulator and connects the two word gates on both outer sides of the two adjacent select gates.

4. The nonvolatile semiconductor memory device as defined in claim 3,

wherein the insulator is formed by extending a material which is the same as the material of the nonvolatile memory element.

5. The nonvolatile semiconductor memory device as defined in claim 1,

wherein the word gate common connection sections are arranged on an imaginary straight line in the column direction.

6. The nonvolatile semiconductor memory device as defined in claim 1, further comprising:

a bitline connection section provided between one of the word gate common connection sections and one of the isolation regions which is adjacent to the word gate common connection section in the row direction,

wherein at least one bitline is connected to one of the bitline diffusion layers through the bitline connection section.